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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/803,084	03/08/2001	Thomas P. Glenn	G0049	8517

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EXAMINER	
WILLIAMS, ALEXANDER O	

ART UNIT	PAPER NUMBER
2826	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/803,084	GLENN ET AL	
	Examiner	Art Unit	
	Alexander O Williams	2826	AW

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 February 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 to 15, 23 to 25 and 30 to 41* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 to 15, 23 to 25 and 30 to 41* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Serial Number: 09/803084 Attorney's Docket #: G0049
Filing Date: 3/8/2001;

Applicant: Glenn et al.

Examiner: Alexander Williams

Applicant's Amendment filed 2/27/04 has been acknowledged.

Claims 16 to 22 and 26 to 29 have been canceled.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(f) or (g) prior art under 35 U.S.C. 103(a).

Claims 1 to 15, 23 to 25 and 30 to 41 are rejected under 35 U.S.C. § 103(a) as being unpatentable Choo et al. (U.S. Patent # 6,407,360).

1. Choo et al. (figures 1 to 37) specifically figures 5 and 20 show a wafer **100** comprising: a first surface **(top of 100)**; a second surface **(bottom of 100)**; a first scribe line **120a** coupled to said first surface, said first scribe line extending in a first direction; a second scribe line **120b** coupled to said first surface, said second scribe line extending in a second direction perpendicular to said first direction; and a first alignment

mark **(127, see figure 20)** formed at an intersection of said first scribe line and said second scribe line. Choo et al. fail to explicitly show said first alignment mark extending from said first surface to said second surface. However, Choo et al. does discloses before cutting the wafer, **pre-cut grooves** at the start edge, end edge, or **cross point of a marked cutting line to selected depth (see figure 5 and column 6, lines 54-58 and column 7, lines 9-18)**.

2. The wafer of Claim 1, Choo et al. further comprising a scribe grid **(intersection of 120a and 120b)** comprising said first scribe line and said second scribe line.

3. The wafer of Claim 2, Choo et al. further comprising electronic components delineated by said scribe grid **(see column 6, lines 59-67)**.

4. The wafer of Claim 3, Choo et al.'s electronic components are selected from the group consisting of integrated circuits, micromachine chips and image sensor chips **(see column 6, lines 59-67)**.

5. The wafer of Claim 3, Choo et al.'s electronic components comprise bond pads coupled to said first surface (inherit).

6. The wafer of Claim 3, Choo et al.'s electronic components comprise active areas coupled to said first surface (inherit).

7. The wafer of Claim 1, Choo et al. further comprising a flat extending in said second direction.

8. The wafer of Claim 1, Choo et al.'s first scribe line delineates a first electronic component from a second electronic component **(see column 6, lines 59-67)**.

9. The wafer of Claim 8, Choo et al.'s second scribe line delineates said second electronic component from a third electronic component **(see column 6, lines 59-67)**.

10. The wafer of Claim 1, Choo et al.'s first alignment mark is an aperture **(see figures 20, and column 6, lines 54-58 and column 7, lines 9-18)**.

11. The wafer of Claim 1, Choo et al. further comprising a first plurality of alignment marks **(intersections of 120a and 120b)** comprising said first alignment mark, said first plurality of alignment marks extending from said first surface to said second surface.

12. The wafer of Claim 11, Choo et al.'s first plurality of alignment marks **(intersections of 120a and 120b)** are aligned with said first scribe line.

13. The wafer of Claim 12, Choo et al. further comprising a second plurality of alignment marks **(intersections of 120a and 120b)** aligned with a third scribe line coupled to said first surface and extending in said second direction.

14. The wafer of Claim 11, Choo et al.'s first plurality of alignment marks **(intersections of 120a and 120b)** define a first line, said first line being aligned with said first scribe line.

15. The wafer of Claim 14, Choo et al. further comprising a second plurality of alignment marks **(intersections of 120a and 120b)** defining a second line, said second line being aligned with a third scribe line coupled to said first surface and extending in said second direction.

23. Choo et al. (figures 1 to 37) specifically figures 5 and 20 show a wafer **100** comprising: a first surface **(top of 100)**; a second surface **(bottom of 100)**; a scribe grid **(120a,120b)** coupled to said first surface; and a plurality of alignment marks **127 (intersection of 120a and 120b).** Choo et al. fail to explicitly show a plurality of

alignment marks extending from said first surface to said second surface, said plurality of alignment marks having a positional relationship to said scribe grid. However, Choo et al. does discloses before cutting the wafer, **pre-cut grooves** at the start edge, end edge, or **cross point of a marked cutting line to selected depth (see figure 5 and column 6, lines 54-58 and column 7, lines 9-18)**.

24. The wafer of Claim 23, Choo et al.'s scribe grid comprises a horizontal scribe line **120a**, a first set of said plurality of alignment marks **127** being aligned with said horizontal scribe line.

25. The wafer of Claim 24, Choo et al.'s scribe grid comprises a vertical scribe line **120b**, a second set of said plurality of alignment marks **127** being aligned with said vertical scribe line.

32. The wafer of Claim 23, Choo et al. further comprising electronic components delineated by said scribe grid **(see column 6, lines 59-67)**.

33. The wafer of Claim 32, Choo et al.'s electronic components are selected from the group consisting of integrated circuits, micromachine chips and image sensor chips **(see column 6, lines 59-67)**.

34. The wafer of Claim 32, Choo et al.'s electronic components comprise bond pads coupled to said first surface (inherit).

35. The wafer of Claim 32, Choo et al.'s electronic components comprise active areas coupled to said first surface (inherit).

36. The wafer of Claim 25, Choo et al.'s vertical scribe line **120b** extends in a first direction and wherein said horizontal scribe line **120a** extends in a second direction, said wafer further comprising a flat extending in said second direction.

37. Choo et al. (figures 1 to 37) specifically figures 5 and 20 show a wafer **100** comprising: a front-side surface **(top surface of 100)**; a back-side surface **(bottom surface of 100)**; a first scribe line **120a,120b** coupled to said front-side surface; and a first back-side alignment mark **(127, see figure 20).** Choo et al. fail to explicitly show a first back-side alignment mark extending from said front-side surface to said back-side surface, said first backside alignment mark being formed along said first scribe line. However, Choo et al. does discloses before cutting the wafer, **pre-cut grooves** at the start edge, end edge, or **cross point of a marked cutting line to selected depth (see figure 5 and column 6, lines 54-58 and column 7, lines 9-18)**.

38. The wafer of Claim 37, Choo et al. further comprising a plurality of back-side alignment marks extending from said front-side surface to said back-side surface, said plurality of back-side alignment marks comprising said first back-side alignment mark (Choo et al. does discloses before cutting the wafer, **pre-cut grooves** at the start edge, end edge, or **cross point of a marked cutting line to selected depth (see figure 5 and column 6, lines 54-58 and column 7, lines 9-18)**.

39. The wafer of Claim 38, Choo et al. plurality of back-side alignment marks **127** have a positional relationship to said first scribe line (Choo et al. does discloses before cutting the wafer, **pre-cut grooves** at the start edge, end edge, or **cross point of a marked cutting line to selected depth (see figure 5 and column 6, lines 54-58 and column 7, lines 9-18)**.

40. Choo et al. (figures 1 to 37) specifically figures 5 and 20 show a wafer **110** comprising: a first surface **(top surface of 100)**; a second surface **(bottom surface of 100)**; a scribe line **120a,120b** coupled to said first surface; and a means **(intersection of 120a and 120b at 127).** Choo et al. Fail to explicitly show a means for determining a position of said scribe line from said second surface, said means for determining extending through said wafer from said first surface to said second surface. However, Choo et al. does discloses before cutting the wafer, **pre-cut grooves** at the start edge, end edge, or **cross point of a marked cutting line to selected depth (see figure 5 and column 6, lines 54-58 and column 7, lines 9-18)**.

Therefore, it would be obvious to one of ordinary skill in the art at the time of the invention to use the teaching of Choo et al.'s depth of groove in a alignment mark to be a hole from a first surface to a second surface for the purpose of providing alignment mark for other procedures can be completed accurately for the completion of making a device.

Initially, and with respect to claims 30 and 31, note that a "product by process" claim is directed to the product per se, no matter how actually made, In re Hirao, 190 USPQ 15 at 17 (footnote 3). See also In re Brown, 173 USPQ 685; In re Luck, 177 USPQ 523; In re Wertheim, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); In re Fitzgerald, 205 USPQ 594, 596 (CCPA); In re Marosi et al., 218 USPQ 289 (CAFC); and most recently, In re Thorpe et al., 227 USPQ 964 (CAFC, 1985) all of which make it clear that it is the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that, as here, an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or not. Note that Applicant has burden of proof in such cases as the above case law makes clear.

As to the grounds of rejection under section 103, see MPEP § 2113.

Response

Applicant's arguments filed 2/27/04 have been fully considered, but are moot in view of the new grounds of rejections detailed above.

The following references are cited as of interest to this application, but not applied at this time.

Field of Search	Date
U.S. Class and subclass: 257/797,620,618,226,59,72,644,650	6/29/03 11/19/03 5/7/04
Other Documentation: foreign patents and literature in 257/797,620,618,226,59,72,644,650	6/29/03 11/19/03 5/7/04
Electronic data base(s): U.S. Patents EAST	6/29/03 11/19/03 5/7/04

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alexander O Williams whose telephone number is (571) 272 1924. The examiner can normally be reached on M-F 6:30-7:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (571) 272 1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

AOW
5/7/04

Alexander Williams
Primary Examiner